

Freeform Search

Database:

US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Term:

 Display: Documents in Display Format: Starting with Number

 Generate: ☐ Hit List ☒ Hit Count ☐ Side by Side ☐ Image

Search

Clear

Interrupt

Search History

 DATE: Friday, May 26, 2006 [Printable Copy](#) [Create Case](#)

Set Name	Query	Hit Count	Set Name
side by side			result set
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
<u>L27</u>	pixel\$1 same first adj refresh rate same second adj refresh adj rate	4	<u>L27</u>
<u>L26</u>	L25 and @py<=2003	17	<u>L26</u>
<u>L25</u>	(display adj element\$1 or pixel\$1) same (first or second) adj refresh adj rate\$1	35	<u>L25</u>
<u>L24</u>	activating adj (display adj element\$1 or pixel\$1) same different adj rate\$1	0	<u>L24</u>
<u>L23</u>	activating adj (display adj element\$1 or pixel\$1) at different adj rate\$1	0	<u>L23</u>
<u>L22</u>	logic adj gate same row adj input same column adj input	1	<u>L22</u>
<u>L21</u>	latch\$6 same row adj input same column adj input	25	<u>L21</u>
<u>L20</u>	L3 addressable adj latch\$1 same signal\$1	0	<u>L20</u>
<u>L19</u>	L3 addressable adj latch\$1 same input\$6	0	<u>L19</u>
<u>L18</u>	L3 addressable adj latch\$1 and row same column	0	<u>L18</u>
<u>L17</u>	L3 addressable adj latch\$1 same row same column	0	<u>L17</u>
<u>L16</u>	L3 addressable adj latch\$1 same row same column	0	<u>L16</u>
<u>L15</u>	L14 and @py<=2003	28	<u>L15</u>
<u>L14</u>	l3 and row same column same input	30	<u>L14</u>

<u>L13</u>	l3 and row same column	65	<u>L13</u>
<u>L12</u>	l3 and row adj address same column address	0	<u>L12</u>
<u>L11</u>	l3 and row adj address same column address same input	0	<u>L11</u>
<u>L10</u>	l9 and logic adj gate adj control\$6 adj switch\$6 same (transistor or TFT or thin adj film adj transistor)	2	<u>L10</u>
<u>L9</u>	L8 and @py<=2003	22	<u>L9</u>
<u>L8</u>	l7 and logic adj gate adj control\$6 adj switch\$6	23	<u>L8</u>
<u>L7</u>	logic adj gate same switch same control\$6	3519	<u>L7</u>
<u>L6</u>	l5 and addressable adj latch\$6 near4 pixel\$1	0	<u>L6</u>
<u>L5</u>	L4 and @py<=2003	20	<u>L5</u>
<u>L4</u>	addressable adj latch\$6 and pixel\$1	23	<u>L4</u>
<u>L3</u>	addressable adj latch\$6	449	<u>L3</u>
<u>L2</u>	addressable adj latch\$6 same pixel\$1	0	<u>L2</u>
<u>L1</u>	(display adj element\$1 or pixels) same addressble adj latch	0	<u>L1</u>

END OF SEARCH HISTORY